ABSTRACT OF THE DISCLOSURE

A bus connection circuit is connected by a bus to a bridge circuit having a plurality of pre-fetch buffers to access memory. A plurality of request queues and a plurality of request signal outputs and grant signal inputs are provided in a single bus connection device. By means of the single bus connection device, a plurality of pre-fetch buffers of a bridge circuit can be utilized effectively, wasted read requests corresponding to retry responses from the bridge circuit can be decreased, and consequently wasted use of a PCI bus can be reduced.